IN THE CLAIMS:

1. (currently amended) An integrated circuit, comprising:
a plurality of interchangeable hard macrocells;
at least one programmable logic block;
a bus intercoupling said plurality of macrocells and said at least one programmable logic block; and
a self-repair program, associated with said at least one programmable logic block, that causes said at least one programmable logic block to test at least some of said plurality of macrocells and place at least a functioning one of said plurality of macrocells into an operational status.

2. (currently amended) The circuit as recited in Claim 1 wherein said plurality of macrocells numbers at least one greater than a required minimum number for operation of said integrated circuit.

3. (original) The circuit as recited in Claim 1 wherein said self-repair program is capable of being dissociated from said at least one programmable logic block to allow said at least one programmable logic block to assume a different function in said integrated circuit.

4. (currently amended) The circuit as recited in Claim 1 wherein said plurality of macrocells are selected from the group consisting of:
random-access memory,
microprocessors,
digital signal processors, and
media access controllers.

5. (currently amended) The circuit as recited in Claim 1 wherein said self-repair program causes said at least one programmable logic block to test all of said plurality of macrocells.

6. (currently amended) The circuit as recited in Claim 1 wherein said self-repair program causes said at least one programmable logic block to employ said bus to test said at least some of said plurality of macrocells.

7. (currently amended) The circuit as recited in Claim 1 further comprising memory that stores a signature for subsequent use to place at least said functioning one of said plurality of macrocells into said operational status, said self-repair program therefore being required only once.

8. (currently amended) A method of manufacturing integrated circuits, comprising:
fabricating a plurality of integrated circuits, each of said integrated circuits including:
a plurality of interchangeable hard macrocells,
at least one programmable logic block, and
a bus intercoupling said plurality of macrocells and said at least one

programmable logic block;

loading a self-repair program into said at least one programmable logic block to cause said at least one programmable logic block to test at least some of said plurality of macrocells and place at least a functioning one of said plurality of macrocells into an operational status; and

employing said self-repair program to grade said plurality of integrated circuits based on a degree of fault-tolerance.

9. (currently amended) The method ~~circuit~~ as recited in Claim 8 wherein said plurality of macrocells numbers at least one greater than a required minimum number for operation of said integrated circuit.

10. (currently amended) The method ~~circuit~~ as recited in Claim 8 wherein said self-repair program is capable of being dissociated from said at least one programmable logic block to allow said at least one programmable logic block to assume a different function in said integrated circuit.

11. (currently amended) The method ~~circuit~~ as recited in Claim 8 wherein said plurality of macrocells are selected from the group consisting of:

random-access memory,

microprocessors,

digital signal processors, and

media access controllers.

12. (currently amended) The method ~~circuit~~ as recited in Claim 8 wherein said self-repair program causes said at least one programmable logic block to test all of said plurality of macrocells.

13. (currently amended) The method ~~circuit~~ as recited in Claim 8 wherein said self-repair program causes said at least one programmable logic block to employ said bus to test said at least some of said plurality of macrocells.

14. (currently amended) The method ~~circuit~~ as recited in Claim 8 further comprising providing a memory that stores a signature for subsequent use to place at least said functioning one of said plurality of macrocells into said operational status, said self-repair program therefore being required only once for each of said plurality of integrated circuits.

15. (currently amended) A method of operating an integrated circuit, comprising:

applying power to a plurality of interchangeable hard macrocells, at least one programmable logic block and a bus, intercoupling said plurality of macrocells and said at least one programmable logic block, that comprise said integrated circuit; and

initiating a self-repair program, associated with said at least one programmable logic block, that causes said at least one programmable logic block to test at least some of said plurality of macrocells and place at least a functioning one of said plurality of macrocells into an operational status.

16. (currently amended) The method as recited in Claim 15 wherein said plurality of macrocells numbers at least one greater than a required minimum number for operation of said integrated circuit.

17. (original) The method as recited in Claim 15 further comprising subsequently dissociating said self-repair program from said at least one programmable logic block to allow said at least one programmable logic block to assume a different function in said integrated circuit.

18. (currently amended) The method as recited in Claim 15 wherein said plurality of macrocells are selected from the group consisting of:

random-access memory,
microprocessors,
digital signal processors, and
media access controllers.

19. (currently amended) The method as recited in Claim 15 wherein said initiating comprises causing said at least one programmable logic block to test all of said plurality of macrocells.

20. (currently amended) The method as recited in Claim 15 wherein said initiating comprises causing said at least one programmable logic block to employ said bus to test said at least some of said plurality of macrocells.

21. (currently amended) The method as recited in Claim 15 further comprising:

storing data into memory; and

retrieving said data subsequently to place at least said functioning one of said plurality of macrocells into said operational status, said initiating being carried out only once.